Chapter 9
Bit Serial Arithmetic

Digit Serial Arithmetic
- Consumes one digit of each operand per cycle
- Produces one digit of the result each cycle

- Two Modes of Operation
  - LSD-First (Least Significant Digit First)
  - MSD-First (Most Significant Digit First)
    - Also called Online Arithmetic
Timing Parameters

- \( r \), the radix
- \( n \), the number of digits input/output
- \( \delta \), the initial delay (online delay)
  - number of addition cycles before first digit is produced
- \( T \), total execution time
  - time from first input digit to last result digit
  - \( T = \delta + n + 1 \)

Serial Addition/Subtraction

**Radix 2**

- LSD-First

**Radix 16**

- LSD-First

Operands:
- \( X \)
- \( Y \)

Result:
- \( Z \)

4-bit ADDER

- \( Z_{0} \)
- \( Z_{1} \)
- \( Z_{2} \)
- \( Z_{3} \)

Carry/borrow FF

(result digit register)
Bit-Srial Multipliers

Dependence Graphs and Regular Array Design

- Show all operations and use arrows to show flow of data between operations.
  - Shows dependences between operations.
- Determine a schedule.
  - What operations can happen at the same time.
- Determine an allocation.
  - What operations can happen in the same place (meaning the same processor).
- Determine communication between processors.
  - Interpret data flow on dependence graph as communication between processors.
Semi-Systolic #1:
A parallel, X serial (LSB first)

Isotemporal line.
Connects operations performed at the same time.

Allocation box.
Encloses operations performed on the same processor.

(4 processors)

AND, full add, latch operation

Same operation, these nodes are used to propagate carries and shift out results.

Semi-systolic Design #1
Requires 4 zeros to be shifted in after the x’s
Modified Design #1

Allows a new problem to be started 4 cycles earlier.

Semi-Systolic #2:
A parallel, X serial (LSB first)
Semi-systolic Design #2

Systolic Design
A parallel, X serial (LSB first)
Systolic Design

A serial and X serial (LSB first)
Bit-Serial Multiplier in Dot Notation

(5:3) Counter Column Reduction

Shift right to obtain \( p^0 \)

Already output

Already accumulated into three numbers

Output

Bit-Serial Multiplier

Winter 2006
ECEn 621 Computer Arithmetic
Dr. Doran Wilde

Bit-Serial Multiplier

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Both Inputs Serial, LSB First (Algebraic Derivation)

Let \[ a^{(i)} = 2^i a_i + a^{(i-1)}, \quad a^{(0)} = a_0 \]
\[ x^{(i)} = 2^i x_i + x^{(i-1)}, \quad x^{(0)} = x_0 \]
\[ m^{(i)} = a^{(i)} x^{(i)} \]
\[ = (2^i a_i + a^{(i-1)})(2^i x_i + x^{(i-1)}) \]
\[ = 2^{2i} a_i x_i + 2^i (a_i x^{(i-1)} + x_i a^{(i-1)}) + a^{(i-1)} x^{(i-1)} \]
\[ = 2^{2i} a_i x_i + 2^i (a_i x^{(i-1)} + x_i a^{(i-1)}) + m^{(i-1)} \]
\[ 2 \cdot 2^{-(i+1)} m^{(i)} = 2^i a_i x_i + a_i x^{(i-1)} + x_i a^{(i-1)} + 2^{-i} m^{(i-1)} \]
\[ 2 p^{(i)} = 2^i a_i x_i + a_i x^{(i-1)} + x_i a^{(i-1)} + p^{(i-1)} \]
Online Arithmetic

- Online arithmetic algorithms operate in a digit-serial MSDF mode
- To compute the first digit of the result, $\delta + 1$ digits of the input operands needed
- Thereafter, for each new digit of the operands, an extra digit of the result obtained
- The online delay $\delta$ typically a small integer, e.g., 1 to 4.

<table>
<thead>
<tr>
<th>Cycle</th>
<th>Input</th>
<th>Compute</th>
<th>Output</th>
</tr>
</thead>
<tbody>
<tr>
<td>-2</td>
<td>$x_1$</td>
<td>$z_1$</td>
<td>$z_1$</td>
</tr>
<tr>
<td>-1</td>
<td>$x_2$</td>
<td>$z_2$</td>
<td>$z_2$</td>
</tr>
<tr>
<td>0</td>
<td>$x_3$</td>
<td>$z_3$</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>$x_4$</td>
<td></td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>$x_5$</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

$\delta = 2$

- The left-to-right mode of computation requires redundancy

Addition/Subtraction Online Arithmetic $r > 2$

The online addition/subtraction algorithm: the serialization of a redundant addition (carry-save or signed-digit)

Radix $r > 2$

$$(t_{j+1}, w_{j+2}) = \begin{cases} (0, x_{j+2} + y_{j+2}) & \text{if } |x_{j+2} + y_{j+2}| \leq a - 1 \\ (1, x_{j+2} + y_{j+2} - r) & \text{if } x_{j+2} + y_{j+2} \geq a \\ (-1, x_{j+2} + y_{j+2} + r) & \text{if } x_{j+2} + y_{j+2} \leq -a \end{cases}$$

and

$$z_{j+1} = w_{j+1} + t_{j+1}$$

where $x_j, y_j, z_j \in \{-a, \ldots, a\}$. 
Addition/Subtraction Online Arithmetic $r > 2$

Digit-parallel radix-2 signed-digit adder converted into a radix-2 online adder with online delay $\delta = 2$

The cycle time is $t_{cy} = 2t_{FA} + t_{FF}$

The operation time $t_{OLADD_{-2}} = (2 + n + 1)t_{cy}$

The cost 2 FAs and 5 FFs.

To reduce the cycle time, pipeline the two stages: reduces the cycle time by one $t_{FA}$ increases online delay to $\delta = 3$. 